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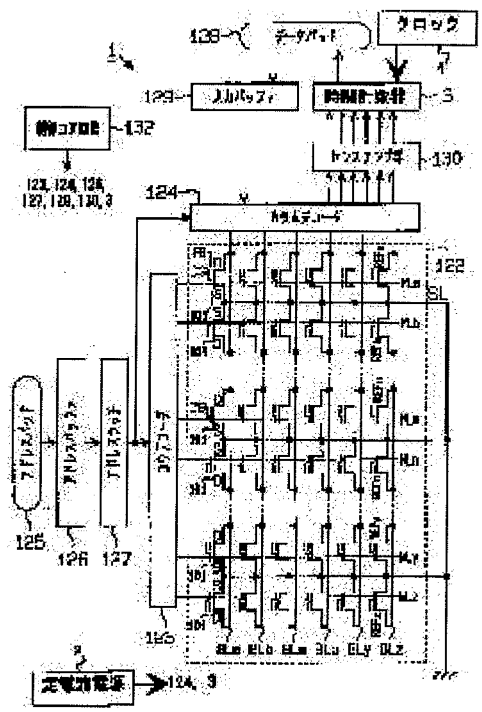
(54) NON-VOLATILE SEMICONDUCTOR MEMORY

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a non-volatile semiconductor memory which assures lower power consumption and provides a sufficient read margin in the read operation.

SOLUTION: At the time of reading data stored in a floating gate FG, the time required from start of impression of a voltage to a control gate CG to actual start of flow of a cell current by a memory cell 101 is counted and the recording data value is judged depending on this counted value. For example, when the recorded time is defined as '0' for under 50ns, '1' for 50ns or more and under 100 ns, '2' for 100ns or more and under 150ns, and '3' for 150ns or more and under 200ns, the recording data can be judged depending on the counted time.



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CLAIMS

[Claim(s)]
[Claim 1] Non-volatile semiconductor memory to which said memory cell carried out counting of the time amount taken to actually begin to pass a cel current, and was characterized by to distinguish a record data value by the size of these enumerated data since it began to have impressed an electrical potential difference to the control gate CG when reading the data currently recorded on the floating gate FG in the non-volatile semiconductor memory which has the memory cell which consists of Source S, and Drain D and Channel CH. [a floating gate FG, the control gate CG, and]
[Claim 2] The non-volatile semiconductor memory which impressed an electrical potential difference to the control gate CG of a reference cel, carried out counting of the time amount until said memory cell begins to pass a cel current since this reference cel began to pass a cel current, and was characterized by to distinguish a record data value by the size of these enumerated data when reading the data currently recorded on the floating gate FG in the non-volatile semiconductor memory which has the memory cell which consists of Source S, and Drain D and Channel CH. [a floating gate FG, the control gate CG, and]
[Claim 3] Non-volatile semiconductor memory characterized by making multiple-value data record on said memory cell, impressing an electrical potential difference to the control gate CG by the constant current power supply in the case of read-out of data, and controlling the potential Vfg of a floating gate FG by controlling the amount of the charge accumulated in said floating gate FG in non-volatile semiconductor memory according to claim 1 or 2 by coupling from the control gate CG.
[Claim 4] Non-volatile semiconductor memory characterized by making multiple-value data record on said memory cell, impressing an electrical potential difference to the control gate CG through the circuit where a time constant is large in the case of read-out of data, and controlling the potential Vfg of a floating gate FG by controlling the amount of the charge accumulated in said floating gate FG in non-volatile semiconductor memory according to claim 1 or 2 by coupling from the control gate CG.
[Claim 5] Non-volatile semiconductor memory characterized by replacing with impressing an electrical potential difference to the control gate CG by the constant current power supply in non-volatile semiconductor memory according to claim 3 or 4, impressing an electrical potential difference to Drain D or Source S by the constant current source, and controlling the potential Vfg of a floating gate FG by Drain D or coupling from Source S.
[Claim 6] Non-volatile semiconductor memory characterized by replacing with impressing an electrical potential difference to the control gate CG through the circuit where a time constant is large in non-volatile semiconductor memory according to claim 3 or 4, impressing an electrical potential difference to Drain D or Source S through the circuit where a time constant is large, and controlling the potential Vfg of a floating gate FG by Drain D or coupling from Source S.
[Claim 7] Non-volatile semiconductor memory characterized by having the number machine of hour meters which carries out counting of the time amount to claim 1 thru/or any 1 term of 6 with a clock in the non-volatile semiconductor memory of a publication.
[Claim 8] Non-volatile semiconductor memory characterized by preparing the control circuit which distinguishes a record data value by the size of gate time in non-volatile semiconductor memory given in claim 1 thru/or any 1 term of 6.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the approach of reading the information on binary or three values or more recorded on the floating gates, such as a flash EEPROM, in detail about a semiconductor nonvolatile memory.
[0002]
[Description of the Prior Art] In recent years, non-volatile semiconductor memory, such as FRAM (Ferro-electric Random Access Memory), EPROM (Erasable and Programmable Read Only Memory), and EEPROM, attracts attention. A charge is accumulated in a floating gate and a data storage is made to perform at EPROM or EEPROM by detecting change of the threshold voltage by the existence of a charge by the control gate. Moreover, there is a flash EEPROM which eliminates data by the whole memory chip, or divides a memory cell array into the block of arbitration, and eliminates data in each of that block unit in EEPROM.
[0003] The memory cell which constitutes a Flash EPROM is roughly classified into a split-gate mold and a stack TOGETO mold.
(Split-gate mold) The flash EEPROM of a split-gate mold is indicated by USP5029130 (G1 1C 11/40).
[0004] The cross-section structure of the split-gate mold memory cell 101 indicated by drawing 5 at this official report is shown. Source S and Drain D of N type are formed on the P type single crystal silicon substrate 102. The floating gate FG is formed through the 1st insulator layer 103 on the channel CH pinched by Source S and Drain D. The control gate CG is formed through the 2nd insulator layer 104 on the floating gate FG. A part of control gate CG is arranged on a channel through the 1st insulator layer 103, and it constitutes the selector gate 105.
[0005] The whole flash EEPROM 121 configuration using the split-gate mold memory cell 101 indicated by drawing 6 at this official report is shown. Two or more memory cells 101 are arranged on a matrix, and the memory cell array 122 is constituted. The control gate CG of each memory cell 101 arranged in the direction of a line (low) is connected to common word line WLa-WLz. The drain D of each memory cell 101 arranged in the direction of a train (column) is connected to common bit line BLa-BL. The source S of all the memory cells 101 is connected to the common source line SL, and the common source line SL is grounded.
[0006] Each word line WLa-WLz is connected to the low decoder 123, and each bit line BLa-BLz is connected to the column decoder 124. The row address and column address which were specified from the outside are inputted into the address pad 125. The row address and column address are transmitted to the address latch 127 through an address buffer 126 from the address pad 125. A row address is transmitted to the low decoder 123 among each address latched by the address latch 127, and a column address is transmitted to the column decoder 124. The low decoder 123 controls the potential of the selected word line corresponding to each mode of operation to choose and carry out the postscript of one word line WLa-WLz corresponding to the row address. The column decoder 124 controls the potential of the selected bit line corresponding to each mode of operation to choose and carry out the postscript of bit line BLa-BLz corresponding to the column address.
[0007] The data specified from the outside are inputted into the data pad 128. The data is transmitted to the column decoder 124 through an input buffer 129 from the data pad 128. The column decoder 124 is controlled to carry out the postscript of the potential of bit line BLa-BLz chosen as mentioned above corresponding to the data. The data read from the memory cell 101 of arbitration are transmitted to the sense amplifier group 130 through the column decoder 124 from bit line BLa-BLz. The sense amplifier group 130 consists of some sense amplifiers (illustration abbreviation). The column decoder 124 connects selected bit line BLa-BLz and each selected sense amplifier. The data distinguished by the sense amplifier group 130 so that a postscript might be carried out are outputted to the exterior through the data pad 128 from an output buffer 131.
[0008] In addition, actuation of each above-mentioned circuit (123, 124, 126, 127,129,130,131) is controlled by the control core circuit 132. Next, each mode of operation (washout mode, a write mode, read-out mode) of a flash EEPROM 121 is explained with reference to drawing 7 a. In addition, also in which mode of operation, the potential of the common source line SL is held at a grand level (=0V).
[0009] (a) In washout mode washout mode, the potential of all bit line BLa-BLz is held at a grand level. 15V are supplied to the selected word line WLm, and potential of other word line (non-choosing word line) WLa-WLl and WLn-WLz is made into a grand level. Therefore, the control gate CG of each memory cell 101 connected to the selected word line WLm is raised by 15V.

[0010] By the way, former one is overwhelmingly large when a floating gate FG, the electrostatic capacity between Drains D, and the electrostatic capacity between the control gate CG and a floating gate FG are measured. Therefore, when the control gate CG is 15V and a drain is 0V, high electric field arise between the control gate CG and a floating gate FG. Consequently, Fowler-Nordheim tunnel current (it is called FN tunnel current Fowler-Nordheim Tunnel Current and the following) flows, the electron in a floating gate FG is drawn out to the control gate CG side, and elimination of the data memorized by the memory cell 101 is performed.
[0011] This elimination actuation is performed to all the memory cells 101 connected to the selected word line WLm. In addition, elimination actuation can also be performed to all the memory cells 101 connected to each of that word line by choosing two or more word line WLa-WLz as coincidence. Thus, the elimination actuation which divides the memory cell array 122 into the block of the arbitration for two or more sets of every word line WLa-WLz, and eliminates data in each of that block unit is called block elimination.
[0012] (b) In a write mode write mode, 1V are supplied to the word line WLm connected to the control gate CG of the selected memory cell 101, and potential of other word line (non-choosing word line) WLa-WLl and WLn-WLz is made into a grand level. 12V are supplied to the bit line BLm connected to the drain D of the selected memory cell 101, and potential of other bit line (non-choosing bit line) BLa-BLl and BLn-BLz is made into a grand level.
[0013] By the way, the threshold voltage Vth of a memory cell 101 is 0.5V. Therefore, in the selected memory cell 101, the control gate CG becomes near threshold voltage Vth, and moves the electron in Source S into the channel CH of weak reversal. On the other hand, since 12V are impressed to Drain D, the potential of a floating gate FG is raised by coupling through the capacity between Drain D and a floating gate FG. Therefore, high electric field arise between the control gate CG and a floating gate FG. Therefore, it is accelerated, and the electron in Channel CH serves as a hot electron, and is poured in to a floating gate FG. Consequently, a charge is accumulated in the floating gate FG of the selected memory cell 101, and 1-bit data are written in and memorized.
[0014] Unlike elimination actuation, this write-in actuation can be performed every selected memory cell 101.
(c) In read-out mode read-out mode, 5V are supplied to the word line WLm connected to the control gate CG of the selected memory cell 101, and potential of other word line (non-choosing word line) WLa-WLl and WLn-WLz is made into a grand level. 2.5V are supplied to the bit line BLm connected to the drain D of the selected memory cell 101, and other bit line (non-choosing bit line) BLa-BLl and BLn-BLz are made into a grand level.
[0015] Since the electron is drawn out out of the floating gate FG of the memory cell 101 in an elimination condition as described above, the floating gate FG has been charged in plus. Moreover, since the electron is poured in all over the floating gate FG of the memory cell 101 in a write-in condition, the floating gate FG has been charged in minus. Therefore, the channel CH directly under floating-gate FG of the memory cell 101 in an elimination condition is turned on, and turns off the channel CH directly under floating-gate FG of the memory cell 101 in a write-in condition. Therefore, when 5V are impressed to the control gate CG, the direction of the memory cell 101 of an elimination condition writes in the current (cel current) which flows from Drain D to Source S, and it becomes larger than the memory cell 101 of a condition.
[0016] By distinguishing the size of the cel current between each of this memory cell 101 with each sense amplifier in the sense amplifier group 130, the value of the data memorized by the memory cell 101 can be read. For example, the value of the data of the memory cell 101 of an elimination condition is read by being referred to as "0" in the value of the data of the memory cell 101 of "1" and a write-in condition. That is, each memory cell 101 can be made to memorize binary [of the data value "1" of an elimination condition, and the data value "0" of a write-in condition].
[0017] Unlike elimination actuation, this read-out actuation can be performed every selected memory cell 101. Incidentally, in the split-gate mold memory cell 101, the flash EEPROM which calls a drain, and a call and Drain D the source for Source S is indicated by WO 92/18980 (G11C 13/00). The potential of each part in each mode of operation in that case is shown in drawing 7 b.
[0018] By the way, in order to raise the degree of integration of a flash EEPROM in recent years, the multiple-value memory write [memory] in a memory cell with an elimination condition, and it was made to make three or more values not only making binary [of a condition] (= 1 bit) memorize but memorize is proposed. The potential Vfg of a floating gate FG and the property of the cel current value Id in the split-gate mold memory cell 101 are shown in drawing 8 . In addition, the floating-gate potential Vfg is the potential of the floating gate FG to Source S.
[0019] In read-out mode, since the constant voltage (=5V) is impressed to the control gate CG, the channel [directly under] CH of the control gate CG functions as constant resistance. Therefore, it can be considered that the split-gate mold memory cell 101 is what carried out series connection of the constant resistance which consists of a floating gate FG, the transistor which consists of the source S and a drain D, and the channel [directly under] CH of the control gate CG.
[0020] Therefore, the floating-gate potential Vfg becomes dominant [the property of a transistor] in the field of under constant value (=3.5V). Therefore, as for the cel current value Id, the floating-gate potential Vfg serves as zero in the field of under the threshold voltage Vth (=0.5V) of a memory cell 101. And when the floating-gate potential Vfg exceeds threshold voltage Vth, the cel current value Id shows an upward property. Moreover, the property of constant resistance which consists of a channel [directly under] CH of the control gate CG becomes dominant, and the cel current Id is saturated with the field in which the floating-gate potential Vfg exceeds 3.5V.
[0021] By the way, the floating-gate potential Vfg is the sum of the potential Vfgw produced with the charge accumulated in the floating gate FG in write-in actuation, and the potential Vfgc produced by coupling from Drain D (Vfg=Vfgw+Vfgc). In read-out actuation, since potential Vfgc is fixed, the cel current value Id is uniquely determined by potential Vfgw. Moreover,

in write-in actuation, the amount of charges of a floating gate FG is controllable by adjusting the operating time. Therefore, in write-in actuation, if potential Vfgw is controlled by adjusting the operating time and controlling the amount of charges of a floating gate FG, the floating-gate potential Vfg is controllable. Consequently, the cel current value Id in read-out actuation can be set as arbitration.
[0022] Then, as shown in drawing 8 , the cel current value Id matches [the field of under 40microA / the field of under 80microA] the field more than a data value "01" and 120microA with a data value "00" for the field of under 120microA a data value "10" and more than 80microA a data value "11" and more than 40microA, respectively. And in write-in actuation, the operating time is adjusted so that the floating-gate potential Vfg (= Va, Vb, Vc) may become a value corresponding to said each cel current value Id (= 40 80,120microA). If it does in this way, one memory cell 101 can be made to memorize the data of four values (= 2 bits).
[0023] However, if each value of data is made equivalent to the cel current value Id, to change of the floating-gate potential Vfg, about the field where change of the cel current value Id is small, the floating-gate potential Vfg will not be determined uniquely, but multiple-value-ization can be performed with the cel current value Id. That is, to change of the floating-gate potential Vfg, since change of the cel current value Id is large, the floating-gate potential Vfg is uniquely determined to the cel current value Id, and two or more data values can be made equivalent to the cel current value Id about the field whose floating-gate potentials Vfg are 0.5-2.5V. However, since the cel current value Id does not change [the floating-gate potential Vfg] to change of the floating-gate potential Vfg about the field less than [0.5V] or beyond 3.5V, the floating-gate potential Vfg is not uniquely determined to the cel current value Id, and two or more data values cannot be made equivalent to the cel current value Id.
[0024] Thus, in the flash EEPROM using the split-gate mold memory cell 101, only a field with much change of the cel current value Id can be used to change of the floating-gate potential Vfg on the occasion of multiple-value-izing.
(Stack TOGETO mold) The cross-section structure of the stack TOGETO mold memory cell 201 is shown in drawing 9 .
[0025] The N type source S and Drain D are formed on the P type single crystal silicon substrate. On the channel CH pinched by Source S and Drain D, the floating gate FG is formed through the 1st insulator layer 203. The control gate CG is formed through the 2nd insulator layer 204 on the floating gate FG. A floating gate FG and the control gate CG are accumulated without shifting mutually. Therefore, Source S and Drain D take symmetry structure to each gates FG and CG and Channel CH.
[0026] The whole flash EEPROM 221 configuration which used the stack TOGETO mold memory cell 201 for drawing 10 is shown. In a flash EEPROM 221, it is the following points to differ from the flash EEPROM 121 using the split-gate mold memory cell 101 shown in drawing 6 R> 6.
[0027] (1) As for the memory cell array 122, two or more memory cells 201 are arranged in the shape of a matrix.
(2) The source S of each memory cell 201 arranged in the direction of a train is connected to common bit line BLa-BLz.
(3) The drain D of all the memory cells 201 is connected to the common drain line DL. The common drain line DL is connected to the common drain line bias circuit 222. The common drain line bias circuit 222 controls the potential of the common drain line DL corresponding to each mode of operation to carry out a postscript. Actuation of the common drain line bias circuit 222 is controlled by the control core circuit 132.
[0028] By the way, in this specification, the name of the source S in the split-gate mold memory cell 101 and the stack TOGETO mold memory cell 201 and Drain D determines read-out actuation as a base, and the one where potential is higher is made to call the source the one where a drain and potential are lower in read-out actuation. And also in write-in actuation or elimination actuation, it is made the same as it in read-out actuation about the name of Source S and Drain D.
[0029] Next, each mode of operation (washout mode, a write mode, read-out mode) of a flash EEPROM 221 is explained with reference to drawing 11 .
(a) In washout mode washout mode, it changes all bit line BLa-BLz into an opening condition, and potential of all the word lines WLm is made into a grand level. The common drain line bias circuit 222 impresses 12V to the drain D of all the memory cells 201 through the common drain line DL.
[0030] Consequently, FN tunnel current flows, the electron in a floating gate FG is drawn out to Drain D side, and elimination of the data indicated by the memory cell 201 is performed. This elimination actuation is performed to all the memory cells 201 connected to the selected word line WLm. In addition, elimination actuation (block elimination) can also be performed so much to all the memory cells 201 connected to each of that word line by choosing two or more word line WLa-WLz as coincidence.
[0031] (b) In a write mode write mode, 12V are supplied to the word line WLm connected to the control gate CG of the selected memory cell 201, and potential of other word line (non-choosing word line) WLa-WLl and WLn-WLz is made into a grand level. 5V are supplied to the bit line BLm connected to the source S of the selected memory cell 201, and potential of other bit line (non-choosing bit line) BLa-BLl and BLn-BLz is made into a grand level. The common drain line bias circuit 222 holds the drain D of all the memory cells 201 to a grand level through the common drain line DL.
[0032] Then, the potential of a floating gate FG is raised by coupling from the control gate CG, and the hot electron generated near the source S is poured in to a floating gate FG. Consequently, a charge is accumulated in the floating gate FG of the selected memory cell 201, and 1-bit data are written in and memorized.
(c) In read-out mode read-out mode, 5V are supplied to the word line WLm connected to the control gate CG of the selected memory cell 201, and potential of other word line (non-choosing word line) WLa-WLl and WLn-WLz is made into a grand level. Potential of all bit line BLa-BLz is made into a grand level. The common drain line bias circuit 222 impresses 5V to

the drain D of all the memory cells 201 through the common drain line DL.
[0033] Consequently, like the case of the split-gate mold memory cell 101, the direction of the memory cell 201 of an elimination condition writes in the current (cel current) which flows from Drain D to Source S, and it becomes larger than the memory cell 201 of a condition. Therefore, each memory cell 201 can be made to memorize binary [of the data value "1" of an elimination condition, and the data value "0" of a write-in condition].
[0034] By the way, multiple-value memory is proposed also by the flash EEPROM using the stack TOGETO mold memory cell 201. The potential Vfg of a floating gate FG and the property of the cel current value Id in the stack TOGETO mold memory cell 201 are shown in drawing 12 . In addition, the floating-gate potential Vfg is the potential of the floating gate FG to Source S.
[0035] In the SUTAKKUTOGE-TO mold memory cell 201, since it is put without a floating gate FG and the control gate CG shifting mutually, the channel [directly under] CH of the control gate CG does not function as constant resistance like the split-gate mold memory cell 101, but it has only the function of a transistor. Therefore, as for the cel current value Id, the floating-gate potential Vfg serves as zero in the field of under the threshold voltage Vth (=1V) of a memory cell 201. And if the floating-gate potential Vfg exceeds threshold voltage Vth, the cel current value Id will become large in proportion to the floating-gate potential Vfg.
[0036] Therefore, if potential Vfgw is controlled by adjusting the operating time and controlling the amount of charges of a floating gate FG also by the stack TOGETO mold memory cell 201 in write-in actuation, the floating-gate potential Vfg is controllable. Consequently, the cel current value Id in read-out actuation can be set as arbitration. Then, as shown in drawing 12 , the cel current value Id matches [the field of under 40microA / the field of under 80microA] the field of under 160microA with a data value "00" for the field of under 120microA a data value "01" and more than 120microA a data value "10" and more than 80microA a data value "11" and more than 40microA, respectively. And in write-in actuation, the operating time is adjusted so that the floating-gate potential Vfg (= Va, Vb, Vc, Vd) may become a value corresponding to said each cel current value Id (= 40 80,120,160microA). If it does in this way, one memory cell 201 can be made to memorize the data of four values (= 2 bits).
[0037] However, in the stack TOGETO mold memory cell 201, even when drawing out a charge from a floating gate FG in elimination actuation, and the charge was extracted too much superfluously and the predetermined electrical potential difference (=0V) for making memory **** 201 into an OFF state is impressed to the control gate CG, Channel CH will turn on. Consequently, a memory cell 201 is always turned on, a cel current flows also in the state of the standby which does not perform each mode of operation (washout mode, a write mode, read-out mode), and the so-called problem of superfluous elimination it becomes impossible to read all the right data values of the memory cell which makes a bit line common arises. Therefore, it is not desirable to use the field of superfluous elimination for a data storage.
[0038] Also in read-out actuation, the sum of the potential Vfgc produced by coupling with the control gate CG and the potential Vfgw produced with the charge accumulated in the floating gate FG determines the potential of a floating gate FG (Vfg=Vfgc+Vfgw). That is, in read-out actuation, the field (Vfg-Vfgc=Vfgw>Vth) where the value which deducted Vfgc from the floating-gate potential Vfg exceeds threshold voltage Vth serves as superfluous elimination in the condition (Vfgc=5V) that the potential of a floating gate FG is raised by 5V by coupling from the control gate CG. That is, when Vfgc is 5V, the field beyond 6V serves as [the floating-gate potential Vfg] superfluous elimination.
[0039] Moreover, if each value of data is made equivalent to the cel current value Id, to change of the floating-gate potential Vfg, about the field where change of the cel current value Id is small, the floating-gate potential Vfg will not be determined uniquely and multiple-value-ization cannot be performed with the cel current value Id. That is, since the cel current value Id does not so much change [the floating-gate potential Vfg] to change of the floating-gate potential Vfg about the field below 1V, the floating-gate potential Vfg is not uniquely determined to the cel current value Id, and two or more data values cannot be made equivalent to the cel current value Id.
[0040] Thus, in the flash EEPROM using the stack TOGETO mold memory cell 201, on the occasion of multiple-value-izing, it cannot push down on change of the floating-gate potential Vfg, and only the field which is a field where change of the cel current value Id is big, and is not superfluous elimination can be used.
[0041]
[Problem(s) to be Solved by the Invention] In order to raise the degree of integration of the memory device per unit area, multiple-value-ization is one of the leading means, and is attracting attention in recent years. In a flash EEPROM, in case a multiple-value cell data is read, the cel current of a read-out cel is compared with a reference current value, and the data values (0, 1, 2, 3 , etc.) recorded on the memory cell are distinguished.
[0042] However, while comparing this reference current with a cel current and having distinguished the record data value, it is required to continue passing the current before and behind 100microper one cel A, and the increment in power consumption is not escaped. Moreover, the more it multiple-value-izes a memory cell, the more, many reference current values for comparing with each value currently recorded must be prepared, the count of a comparison with a reference current value increases, the read-out time amount per cel becomes long, and there is a problem which cannot respond to improvement in the speed.
[0043] On the other hand, in order to carry out write-in read-out of data to stability correctly and to prevent incorrect writing and incorrect read-out, it is desirable to prepare sufficient margin (large tolerance) in the range of the floating-gate potential Vfg corresponding to each data value of a multiple value and the range of the cel current value Id. However, as described above, by the flash EEPROM of a type, change of the cel current value Id can use only a big field to change of the floating-

gate potential Vfg on the occasion of multiple-value-izing conventionally. Therefore, it is difficult to take sufficient margin for the range of the floating-gate potential Vfg corresponding to each data value of a multiple value, and the cel current value Id.
[0044] For example, in the split-gate mold memory cell 101 shown in drawing 8 , the range of the cel current value Id corresponding to each data value is 40microA, and the range of the floating-gate potential Vfg corresponding to 0.5V and a data value "01" in the range of the floating-gate potential Vfg corresponding to a data value "10" is 1V. Moreover, in the stack TOGETO mold memory cell 201 shown in drawing 12 , the range of the cel current value Id corresponding to each data value is 40microA, and the range of the floating-gate potential Vfg is 1.25V.
[0045] Thus, if the range of the floating-gate potential Vfg corresponding to each data value is narrow, in write-in actuation, there are few margins, it becomes difficult to set up the floating-gate potential Vfg in tolerance correctly, and since there are few margins, incorrect read-out will tend to occur also in read-out actuation. This problem appears more notably as multiple-value-ization progresses, and in an octal or 16 values, margin reservation of write-in read-out actuation becomes still more difficult [the part to which the range of the floating-gate potential Vfg corresponding to each data value of a multiple value and the range of the cel current value Id become narrow] compared with the case of four values.
[0046] If supply voltage is raised only for the purpose of securing a margin on the other hand, the upper limit of Vfg is raised and the upper limit of a cel current value is raised, in the case of read-out, a sense amplifier will detect the data value of a cel for much more currents with a sink, and the problem of the above-mentioned increment in power consumption will be promoted further. It is made in order that this invention may solve the above-mentioned trouble, and the purpose is in offering the non-volatile semiconductor memory which can secure read-out margin with it in read-out actuation. [small and power consumption and] [sufficient]
[0047]
[Means for Solving the Problem] It has the memory cell which consists of Source S, and Drain D and Channel CH if it is in the non-volatile semiconductor memory of claim 1, and since it begins to impress an electrical potential difference to the control gate CG in case the data currently recorded on the floating gate FG are read, said memory cell carries out counting of the time amount taken to actually begin to pass a cel current, and distinguishes a record data value by the size of these enumerated data. [a floating gate FG, the control gate CG, and]
[0048] That is, counting of the time amount which takes read-out of data for the potential of the floating gate to rise and for a read-out memory cell to actually begin to pass a cel current since an electrical potential difference begins to be impressed to a floating gate FG is carried out. for example, this recorded time amount -- 50ns or more, "2" can be distinguished for "1" and less than 150ns 100ns or more, and record data can be distinguished [less than 50ns / "0" and less than 100ns] for less than 200ns 150ns or more by "3", then the size of time amount by which counting was carried out.
[0049] Moreover, if it is in the non-volatile semiconductor memory of claim 2 It is what has the memory cell which consists of Source S, and Drain D and Channel CH. [a floating gate FG, the control gate CG, and] In case the data currently recorded on the floating gate FG are read, an electrical potential difference is impressed to the control gate CG of a reference cel. Since this reference cel begins to pass a cel current, counting of the time amount until said memory cell begins to pass a cel current is carried out, and a record data value is distinguished by the size of these enumerated data.
[0050] That is, since an electrical potential difference begins to be impressed to a floating gate FG, the potential of the floating gate FG of a reference cel rises, and since a reference cel begins to pass a cel current, read-out of data carries out counting of the time amount until the memory cell which carries out the control gate CG to a reference cel in common begins to pass a cel current. By carrying out like this, the time variation which the channel generation resulting from process dispersion, such as gate processing, takes can be effectively removed from the error of data detection.
[0051] and these enumerated data -- for example, 0 or 50ns or more, less than 150ns can be distinguished 1,100ns or more, and a record data value can be distinguished [less than 50ns / less than 100ns] for less than 200ns 2,150ns or more by 3, then the size of time amount by which counting was carried out. Moreover, if it is in the non-volatile semiconductor memory of claim 3, it is controlling the amount of the charge accumulated in said floating gate FG, and multiple-value data are made to record on said memory cell, in the case of read-out of data, an electrical potential difference is impressed to the control gate CG by the constant current power supply, and the potential Vfg of a floating gate FG is controlled by coupling from the control gate CG.
[0052] That is, in read-out mode, the amount of the current which flows into the control gate CG from a constant current power supply is adjusted, and it controls so that the potential R/C per time amount of the control gate CG becomes small. Moreover, if it is in the non-volatile semiconductor memory of claim 4, it is controlling the amount of the charge accumulated in said floating gate FG, and multiple-value data are made to record on said memory cell, in the case of read-out of data, an electrical potential difference is impressed to the control gate CG through the circuit where a time constant is large, and the potential Vfg of a floating gate FG is controlled by coupling from the control gate CG.
[0053] That is, in read-out mode, when a time constant with strong resistance lets the circuit beyond about 1000ns and it pass and carries out electrical-potential-difference impression, it controls so that the potential R/C per time amount of the control gate CG becomes small. moreover -- a claim -- five -- a non-volatile -- semiconductor memory -- it is -- if -- being according to claim 3 or 4 -- a non-volatile -- semiconductor memory -- setting -- the time -- a constant current power supply -- control -- the gate -- CG -- an electrical potential difference -- impressing -- things -- replacing with -- a constant current source -- a drain -- D -- or -- the source -- S -- an electrical potential difference -- impressing -- a drain -- D -- or -- the source -- S -- from -- coupling -- a floating gate -- FG -- potential -- Vfg -- controlling -- a thing -- it is .

[0054] Moreover, if it is in the non-volatile semiconductor memory of claim 6, in non-volatile semiconductor memory according to claim 3 or 4, a time constant replaces with impressing an electrical potential difference to the control gate CG through a large circuit, impresses an electrical potential difference to Drain D or Source S through the circuit where a time constant is large, and controls the potential Vfg of a floating gate FG by Drain D or coupling from Source S.
[0055] Moreover, if it is in the non-volatile semiconductor memory of claim 7, the number machine of hour meters which carries out counting of the time amount with a clock is formed. Moreover, if it is in the non-volatile semiconductor memory of claim 8, the control circuit which distinguishes a record data value by the size of gate time is prepared.
[0056]
[Embodiment of the Invention] Below, the operation gestalt which materialized this invention is explained according to a drawing.
(The 1st operation gestalt) The 1st operation gestalt which materialized this invention is explained based on a drawing. The whole flash EEPROM configuration which used the split-gate mold memory cell 101 of this operation gestalt for drawing 1 is shown. One memory cell 101 can be made to memorize the data beyond 4 values (= 2 bits) in this operation gestalt.
[0057] In drawing 1 , it is the point of the following related with read-out that a flash EEPROM 1 differs from the conventional flash EEPROM 121 shown in drawing 6 . There are not the conventional example and a difference about the part about washout mode and a write mode.
(1) In read-out mode, in case an electrical potential difference is impressed to Drain D by the column decoder, carry out using a constant current power supply 2. In other modes, this constant current power supply 2 is bypassed, and electrical-potential-difference impression is performed.
[0058] (2) In read-out mode, the number machine 3 of hour meters is used as an output buffer. This forms the counter 2 bits or more for every bit line, and carries out counting of the time difference with the time of day when it reads at with the time of day which impressed the electrical potential difference with the common clock 4, and a memory cell begins to pass a current. The cross-section structure of the split-gate mold memory cell in this operation gestalt is the same as that of what was shown in drawing 5 . A constant current source 2 is connected to Drain D in the case of read-out, and it raises the potential of Drain D with time amount. At this time, the potential Vfg of a floating gate FG also rises with time amount by coupling from Drain D. If the potential Vfg of a floating gate exceeds the threshold voltage Vth of a memory cell, Channel CH will be generated under a floating gate and a cel current will begin to flow.
[0059] With this operation gestalt, since the capacity Ccf of the control gate CG and a floating gate FG is very small compared with the capacity of Drain D and a floating gate FG, and the capacity of a floating gate FG and a substrate, it disregards this and continues explanation below. It reads with Drain D and capacity between Cdf, a floating gate FG, and a substrate (just before channel generation) is set to Cfs for the capacity between the floating gates FG of a memory cell. By coupling with Drain D Set to QdfQfs positive charge accumulated in capacity Cdf and Cfs, respectively, and if the potential difference of Vfg, a floating gate, and a substrate is set to Vfs for the potential of Vd and a floating gate, the potential of Drain D A channel is generated when the potential Vfg of a floating gate FG becomes equal to Vth like following the (1) type.
[0060]
Vfg=Vth=Vfs=Vd-Vdf ---(1)
In this invention, the time amount t which this took is measured and the written-in data value is distinguished. That is, it is an electron (negative charge) to a floating gate FG by the writing of data. - When a channel is generated, it becomes Vdf=(Qw+Qdf)/CdfVfs=Vth=Vfg=Qfs/CfsQdf=Qfs, therefore Vd=Vdf+Vth=(Qw+Qdf)/Cdf+Qfs/Cfs, and compared with the case where there is no are recording of a charge in floating-gate CG, where Qw is accumulated, if only Qw/Cdf does not give big potential to the control gate CG, channel generation will not take place but channel generation will take time amount only at this rate. For this reason, if positive charge is given to Drain D in proportion to time amount and the potential of the control gate CG is raised using the constant current power supply 2, the amount of the electron accumulated by data writing will be uniquely detected by the time amount which channel generation takes.
[0061] for example, the case where the data of four values are distinguished -- time amount t<a a case -- "00" and a<t<b it is -- a case -- "01" and b<t<c it is -- a case -- "10" and t>b it is -- the case specifies beforehand that it calls it "11" (a<b<c<d), and carries out a comparison test in the control core circuit 132.
(The 2nd operation gestalt) The 2nd operation gestalt which materialized this invention is explained based on a drawing.
[0062] In this operation gestalt, differing from the 1st operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 1st operation gestalt.
(1) In read-out mode, in case an electrical potential difference is impressed to Drain D by the column decoder 124, as it replaces with a constant current power supply 2 and is shown in drawing 2 , it lets the circuit 5 where a time constant is big pass, and carry out using the usual constant voltage power supply 6. In other modes, the circuit 5 where this time constant is big is bypassed, and electrical-potential-difference impression is performed.
[0063] Namely, output voltage of a constant voltage power supply V0 and time constant of a circuit 5 tau Then, the drain electrical potential difference Vd in read-out mode becomes Vcg = V0[1-exp(- t/tau)] (for a time constant and t, time amount and V0 are [tau] supply voltage). Big Resistance R and capacity C are contained in the circuit 5 where a time constant is big, and the time constant has become more than 1000ns or it. Thus, if an electrical potential difference is impressed to Drain D through a circuit with a big time constant, the power surge per time amount can be made small, and a gradually big electrical potential difference will be impressed to Drain D with the passage of time. Thus, by using the circuit 5 where a time

constant is big, the voltage buildup rate of the drain D per time amount can be made small, before a read-out memory cell reaches threshold voltage so that there are many electrons accumulated in the floating gate by data writing like the 1st operation gestalt in this case, time amount can be taken mostly, and the data value written in by carrying out counting of this time amount can be distinguished.
(The 3rd operation gestalt) The 3rd operation gestalt which materialized this invention is explained below.
[0064] In this operation gestalt, differing from the 1st operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 1st operation gestalt.
(1) In read-out mode, only the number of the cel read to coincidence forms the counter 2 bits or more in the number machine 3 of hour meters used as an output buffer, and carry out counting of the time difference of the time of day which impressed the electrical potential difference to the drain D of a read-out memory cell, and the time of day when a read-out memory cell begins to pass a current to it using the signal of the common clock 4.
[0065] Therefore, since it is sufficient for the number of a counter if only the number of the input output line of data is prepared, and it does not need to attach a counter to all bit lines, a circuit is made as for it to an abbreviation and a small scale.
(The 4th operation gestalt) The 4th operation gestalt which materialized this invention is explained based on a drawing. In this operation gestalt, differing from the 1st operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 1st operation gestalt.
[0066] (1) Prepare every one reference cel REFa-REFz for detecting a reference sign for every word line in drawing 1 . For example, a cel connected to the bit line BLz is made into reference cel REFa-REFz. From the time of day when this cel began to pass a cel current, a read-out memory cell carries out counting of the time difference by the time of day which begins to pass a cel current with the number vessel 5 of hour meters using the signal of a clock 4.
[0067] When it carries out like this, read-out of data by coupling from Drain D An electrical potential difference is impressed to a floating gate FG, and the potential of the floating gate FG of a reference cel rises. By the signal which began to pass a cel current, the read-out memory cell to which a reference cel starts counting with a clock by the signal which began to pass a cel current, and carries out the control gate CG to a reference cel in common measures a stop and two kinds of this time difference, and records counting with a clock. In this way, even if there is process dispersion, such as gate processing, the time variation which the channel generation resulting from this takes can be effectively removed from the error of data detection.
(The 5th operation gestalt) The 5th operation gestalt which materialized this invention is explained based on a drawing.
[0068] The whole flash EEPROM configuration which used the stack TOGETO mold memory cell 201 of this operation gestalt for drawing 3 is shown. One memory cell 201 can be made to memorize the data beyond 4 values (= 2 bits) in this operation gestalt. In drawing 3 , it is the point of the following related with read-out that a flash EEPROM 2 differs from the conventional flash EEPROM 221 shown in drawing 10 . About the part about washout mode and a write mode, it is the same as that of the conventional example.
[0069] (1) In read-out mode, in case an electrical potential difference is impressed to the control gate by the low decoder 123, carry out using a constant current power supply 2. In other modes, this constant current power supply 2 is bypassed, and electrical-potential-difference impression is performed.
(2) In read-out mode, the number machine 3 of hour meters is used as an output buffer. This forms the counter 2 bits or more for every bit line, and carries out counting of the time difference with the time of day when it reads at with the time of day which impressed the electrical potential difference with the common clock 4, and a memory cell begins to pass a current.
[0070] The cross-section structure of the stack TOGETO mold memory cell in this operation gestalt is the same as that of what was shown in drawing 9 . A constant current power supply 151 is connected with the control gate CG in the case of read-out, and it raises the potential of the control gate CG with time amount. At this time, the potential Vfg of a floating gate FG also rises with time amount by coupling from the control gate CG. If the potential Vfg of a floating gate exceeds the threshold voltage Vth of a memory cell 201, Channel CH will be generated and a cel current will begin to flow.
[0071] It reads with the control gate CG and capacity between Ccf, a floating gate FG, and a substrate (just before channel generation) is set to Cfs for the capacity between the floating gates FG of a memory cell. By coupling with the control gate CG Positive charge accumulated in capacity Ccf and Cfs is set to QcfQfs, respectively. A channel is generated, when it becomes about the potential of Vcg and a floating gate in the potential of the control gate and Vfs, then the potential Vfg of a floating gate FG become equal to Vth like following the (2) type about the potential difference of Vcf, a floating gate, and a substrate in the potential difference of Vfg, the control gate, and a floating gate.
[0072]
Vfg=Vth=Vfs=Vcg-Vcf ---(2)
In this invention, the time amount t which this took is measured and the written-in data value is distinguished. That is, it is an electron (negative charge) to floating-gate CG by the writing of data. - When a channel is generated, it becomes Vcf= (Qw+Qcf)/CcfVfs=Vth=Vfg=Qfs/CfsQcf=Qfs, therefore Vcg=Vcf+Vth=(Qw+Qcf)/Ccf+Qfs/Cfs, and compared with the case where there is no are recording of a charge in floating-gate CG, where Qw is accumulated, if only Qw/Ccf does not give big potential to the control gate CG, channel generation will not take place but channel generation will take time amount only at this rate. For this reason, if positive charge is given to the control gate CG in proportion to time amount and the potential of the control gate CG is raised using the constant current power supply 2, the amount of the electron accumulated by data writing will be uniquely detected by the time amount which channel generation takes.

[0073] for example, the case where the data of four values are distinguished -- time amount t<a a case -- "00" and a<t<b it is -- a case -- "01" and b<t<c it is -- a case -- "10" and t>b it is -- the case specifies beforehand that it calls it "11" (a<b<c<d), and carries out a comparison test in the control core circuit 132.
(The 6th operation gestalt) The 6th operation gestalt which materialized this invention is explained based on a drawing.
[0074] In this operation gestalt, differing from the 5th operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 5th operation gestalt.
(1) In read-out mode, in case an electrical potential difference is impressed to the control gate FG by the low decoder 123, it lets the circuit 5 where the time constant shown in drawing 4 is big pass, and carry out using the usual constant voltage power supply 6. In other modes, the circuit 5 where this time constant is big is bypassed, and electrical-potential-difference impression is performed.
[0075] That is, the control gate voltage [in / for the time constant of V0 and a circuit 5 / in the output voltage of a constant voltage power supply / tau, then read-out mode] Vcg becomes Vcg = V0[1-exp(- t/tau)] (for a time constant and t, time amount and V0 are [tau] supply voltage). Big Resistance R and capacity C are contained in the circuit 5 where a time constant is big, and the time constant has become more than 1000ns or it. Thus, if an electrical potential difference is impressed to Drain D through a circuit with a big time constant, the power surge per time amount can be made small, and a gradually big electrical potential difference will be impressed to Drain D with the passage of time. Thus, by using the circuit 5 where a time constant is big, the voltage buildup rate of the drain D per time amount can be made small, before a read-out memory cell reaches threshold voltage so that there are many electrons accumulated in the floating gate by data writing like the 5th operation gestalt in this case, time amount can be taken mostly, and the data value written in by carrying out counting of this time amount can be distinguished.
(The 7th operation gestalt) The 7th operation gestalt which materialized this invention is explained below.
[0076] In this operation gestalt, differing from the 5th operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 5th operation gestalt.
(1) In read-out mode, only the number of the cel read to coincidence forms the counter 2 bits or more in the number machine 3 of hour meters used as an output buffer, and carry out counting of the time difference of the time of day which impressed the electrical potential difference to the control gate CG of a read-out memory cell, and the time of day when a read-out memory cell begins to pass a current to it using the signal of the common clock 4.
[0077] Therefore, since it is sufficient for the number of a counter if only the number of the input output line of data is prepared, and it does not need to attach a counter to all bit lines, it omits a circuit and is made on a small scale.
(The 8th operation gestalt) The 8th operation gestalt which materialized this invention is explained based on a drawing. In this operation gestalt, differing from the 5th operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 5th operation gestalt.
[0078] (1) Prepare every one reference cel REFa-REFz for detecting a reference sign for every word line in drawing 3 . For example, a cel connected to the bit line BLz is made into reference cel REFa-REFz. From the time of day when this cel began to pass a cel current, a read-out memory cell carries out counting of the time difference by the time of day which begins to pass a cel current with the number vessel 5 of hour meters using the signal of a clock 4.
[0079] When it carries out like this, read-out of data by coupling from the control gate CG An electrical potential difference is impressed to a floating gate FG, and the potential of the floating gate FG of a reference cel rises. By the signal which began to pass a cel current, the read-out memory cell to which a reference cel starts counting with a clock by the signal which began to pass a cel current, and carries out the control gate CG to a reference cel in common measures a stop and two kinds of this time difference, and records counting with a clock. In this way, even if there is process dispersion, such as gate processing, the time variation which the channel generation resulting from this takes can be effectively removed from the error of data detection.
[0080]
[Effect of the Invention] If it is in the non-volatile semiconductor memory of this invention, since it is possible to secure sufficient read-out margin in readout actuation of the data of the memory cell which made the multiple-value data of binary or three values or more memorize, data can be read correctly.
[0081] Moreover, since multiple-value data can be distinguished without hardly passing a cel current, it is possible to supply non-volatile semiconductor memory with little power consumption. And package read-out can do many cels according to there being little power consumption, and improvement in a data read-out rate is possible.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] This invention relates to the approach of reading the information on binary or three values or more recorded on the floating gates, such as a flash EEPROM, in detail about a semiconductor nonvolatile memory.

[Translation done.]

PRIOR ART

[Description of the Prior Art] In recent years, non-volatile semiconductor memory, such as FRAM (Ferro-electric Random Access Memory), EPROM (Erasable and Programmable Read Only Memory), and EEPROM, attracts attention. A charge is accumulated in a floating gate and a data storage is made to perform at EPROM or EEPROM by detecting change of the threshold voltage by the existence of a charge by the control gate. Moreover, there is a flash EEPROM which eliminates data by the whole memory chip, or divides a memory cell array into the block of arbitration, and eliminates data in each of that block unit in EEPROM.
[0003] The memory cell which constitutes a Flash EPROM is roughly classified into a split-gate mold and a stack TOGETO mold.
(Split-gate mold) The flash EEPROM of a split-gate mold is indicated by USP5029130 (G1 1C 11/40).
[0004] The cross-section structure of the split-gate mold memory cell 101 indicated by drawing 5 at this official report is shown. Source S and Drain D of N type are formed on the P type single crystal silicon substrate 102. The floating gate FG is formed through the 1st insulator layer 103 on the channel CH pinched by Source S and Drain D. The control gate CG is formed through the 2nd insulator layer 104 on the floating gate FG. A part of control gate CG is arranged on a channel through the 1st insulator layer 103, and it constitutes the selector gate 105.
[0005] The whole flash EEPROM 121 configuration using the split-gate mold memory cell 101 indicated by drawing 6 at this official report is shown. Two or more memory cells 101 are arranged on a matrix, and the memory cell array 122 is constituted. The control gate CG of each memory cell 101 arranged in the direction of a line (low) is connected to common word line WLa-WLz. The drain D of each memory cell 101 arranged in the direction of a train (column) is connected to common bit line BLa-BL. The source S of all the memory cells 101 is connected to the common source line SL, and the common source line SL is grounded.
[0006] Each word line WLa-WLz is connected to the low decoder 123, and each bit line BLa-BLz is connected to the column decoder 124. The row address and column address which were specified from the outside are inputted into the address pad 125. The row address and column address are transmitted to the address latch 127 through an address buffer 126 from the address pad 125. A row address is transmitted to the low decoder 123 among each address latched by the address latch 127, and a column address is transmitted to the column decoder 124. The low decoder 123 controls the potential of the selected word line corresponding to each mode of operation to choose and carry out the postscript of one word line WLa-WLz corresponding to the row address. The column decoder 124 controls the potential of the selected bit line corresponding to each mode of operation to choose and carry out the postscript of bit line BLa-BLz corresponding to the column address.
[0007] The data specified from the outside are inputted into the data pad 128. The data is transmitted to the column decoder 124 through an input buffer 129 from the data pad 128. The column decoder 124 is controlled to carry out the postscript of the potential of bit line BLa-BLz chosen as mentioned above corresponding to the data. The data read from the memory cell 101 of arbitration are transmitted to the sense amplifier group 130 through the column decoder 124 from bit line BLa-BLz. The sense amplifier group 130 consists of some sense amplifiers (illustration abbreviation). The column decoder 124 connects selected bit line BLa-BLz and each selected sense amplifier. The data distinguished by the sense amplifier group 130 so that a postscript might be carried out are outputted to the exterior through the data pad 128 from an output buffer 131.
[0008] In addition, actuation of each above-mentioned circuit (123, 124, 126, 127,129,130,131) is controlled by the control core circuit 132. Next, each mode of operation (washout mode, a write mode, read-out mode) of a flash EEPROM 121 is explained with reference to drawing 7 a. In addition, also in which mode of operation, the potential of the common source line SL is held at a grand level (=0V).
[0009] (a) In washout mode washout mode, the potential of all bit line BLa-BLz is held at a grand level. 15V are supplied to the selected word line WLm, and potential of other word line (non-choosing word line) WLa-WLl and WLn-WLz is made into a grand level. Therefore, the control gate CG of each memory cell 101 connected to the selected word line WLm is raised by 15V.
[0010] By the way, former one is overwhelmingly large when a floating gate FG, the electrostatic capacity between Drains D, and the electrostatic capacity between the control gate CG and a floating gate FG are measured. Therefore, when the control gate CG is 15V and a drain is 0V, high electric field arise between the control gate CG and a floating gate FG. Consequently, Fowler-Nordheim tunnel current (it is called FN tunnel current Fowler-Nordheim Tunnel Current and the following) flows, the electron in a floating gate FG is drawn out to the control gate CG side, and elimination of the data memorized by the

memory cell 101 is performed.
[0011] This elimination actuation is performed to all the memory cells 101 connected to the selected word line WLm. In addition, elimination actuation can also be performed to all the memory cells 101 connected to each of that word line by choosing two or more word line WLa-WLz as coincidence. Thus, the elimination actuation which divides the memory cell array 122 into the block of the arbitration for two or more sets of every word line WLa-WLz, and eliminates data in each of that block unit is called block elimination.
[0012] (b) In a write mode write mode, 1V are supplied to the word line WLm connected to the control gate CG of the selected memory cell 101, and potential of other word line (non-choosing word line) WLa-WLl and WLn-WLz is made into a grand level. 12V are supplied to the bit line BLm connected to the drain D of the selected memory cell 101, and potential of other bit line (non-choosing bit line) BLa-BLl and BLn-BLz is made into a grand level.
[0013] By the way, the threshold voltage Vth of a memory cell 101 is 0.5V. Therefore, in the selected memory cell 101, the control gate CG becomes near threshold voltage Vth, and moves the electron in Source S into the channel CH of weak reversal. On the other hand, since 12V are impressed to Drain D, the potential of a floating gate FG is raised by coupling through the capacity between Drain D and a floating gate FG. Therefore, high electric field arise between the control gate CG and a floating gate FG. Therefore, it is accelerated, and the electron in Channel CH serves as a hot electron, and is poured in to a floating gate FG. Consequently, a charge is accumulated in the floating gate FG of the selected memory cell 101, and 1-bit data are written in and memorized.
[0014] Unlike elimination actuation, this write-in actuation can be performed every selected memory cell 101.
(c) In read-out mode read-out mode, 5V are supplied to the word line WLm connected to the control gate CG of the selected memory cell 101, and potential of other word line (non-choosing word line) WLa-WLl and WLn-WLz is made into a grand level. 2.5V are supplied to the bit line BLm connected to the drain D of the selected memory cell 101, and other bit line (non-choosing bit line) BLa-BLl and BLn-BLz are made into a grand level.
[0015] Since the electron is drawn out out of the floating gate FG of the memory cell 101 in an elimination condition as described above, the floating gate FG has been charged in plus. Moreover, since the electron is poured in all over the floating gate FG of the memory cell 101 in a write-in condition, the floating gate FG has been charged in minus. Therefore, the channel CH directly under floating-gate FG of the memory cell 101 in an elimination condition is turned on, and turns off the channel CH directly under floating-gate FG of the memory cell 101 in a write-in condition. Therefore, when 5V are impressed to the control gate CG, the direction of the memory cell 101 of an elimination condition writes in the current (cel current) which flows from Drain D to Source S, and it becomes larger than the memory cell 101 of a condition.
[0016] By distinguishing the size of the cel current between each of this memory cell 101 with each sense amplifier in the sense amplifier group 130, the value of the data memorized by the memory cell 101 can be read. For example, the value of the data of the memory cell 101 of an elimination condition is read by being referred to as "0" in the value of the data of the memory cell 101 of "1" and a write-in condition. That is, each memory cell 101 can be made to memorize binary [of the data value "1" of an elimination condition, and the data value "0" of a write-in condition].
[0017] Unlike elimination actuation, this read-out actuation can be performed every selected memory cell 101. Incidentally, in the split-gate mold memory cell 101, the flash EEPROM which calls a drain, and a call and Drain D the source for Source S is indicated by WO 92/18980 (G11C 13/00). The potential of each part in each mode of operation in that case is shown in drawing 7 b.
[0018] By the way, in order to raise the degree of integration of a flash EEPROM in recent years, the multiple-value memory write [memory] in a memory cell with an elimination condition, and it was made to make three or more values not only making binary [of a condition] (= 1 bit) memorize but memorize is proposed. The potential Vfg of a floating gate FG and the property of the cel current value Id in the split-gate mold memory cell 101 are shown in drawing 8 . In addition, the floating-gate potential Vfg is the potential of the floating gate FG to Source S.
[0019] In read-out mode, since the constant voltage (=5V) is impressed to the control gate CG, the channel [directly under] CH of the control gate CG functions as constant resistance. Therefore, it can be considered that the split-gate mold memory cell 101 is what carried out series connection of the constant resistance which consists of a floating gate FG, the transistor which consists of the source S and a drain D, and the channel [directly under] CH of the control gate CG.
[0020] Therefore, the floating-gate potential Vfg becomes dominant [the property of a transistor] in the field of under constant value (=3.5V). Therefore, as for the cel current value Id, the floating-gate potential Vfg serves as zero in the field of under the threshold voltage Vth (=0.5V) of a memory cell 101. And when the floating-gate potential Vfg exceeds threshold voltage Vth, the cel current value Id shows an upward property. Moreover, the property of constant resistance which consists of a channel [directly under] CH of the control gate CG becomes dominant, and the cel current Id is saturated with the field in which the floating-gate potential Vfg exceeds 3.5V.
[0021] By the way, the floating-gate potential Vfg is the sum of the potential Vfgw produced with the charge accumulated in the floating gate FG in write-in actuation, and the potential Vfgc produced by coupling from Drain D (Vfg=Vfgw+Vfgc). In read-out actuation, since potential Vfgc is fixed, the cel current value Id is uniquely determined by potential Vfgw. Moreover, in write-in actuation, the amount of charges of a floating gate FG is controllable by adjusting the operating time. Therefore, in write-in actuation, if potential Vfgw is controlled by adjusting the operating time and controlling the amount of charges of a floating gate FG, the floating-gate potential Vfg is controllable. Consequently, the cel current value Id in read-out actuation can be set as arbitration.
[0022] Then, as shown in drawing 8 , the cel current value Id matches [the field of under 40microA / the field of under

80microA] the field more than a data value "01" and 120microA with a data value "00" for the field of under 120microA a data value "10" and more than 80microA a data value "11" and more than 40microA, respectively. And in write-in actuation, the operating time is adjusted so that the floating-gate potential Vfg (= Va, Vb, Vc) may become a value corresponding to said each cel current value Id (= 40 80,120microA). If it does in this way, one memory cell 101 can be made to memorize the data of four values (= 2 bits).
[0023] However, if each value of data is made equivalent to the cel current value Id, to change of the floating-gate potential Vfg, about the field where change of the cel current value Id is small, the floating-gate potential Vfg will not be determined uniquely, but multiple-value-ization can be performed with the cel current value Id. That is, to change of the floating-gate potential Vfg, since change of the cel current value Id is large, the floating-gate potential Vfg is uniquely determined to the cel current value Id, and two or more data values can be made equivalent to the cel current value Id about the field whose floating-gate potentials Vfg are 0.5-2.5V. However, since the cel current value Id does not change [the floating-gate potential Vfg] to change of the floating-gate potential Vfg about the field less than [0.5V] or beyond 3.5V, the floating-gate potential Vfg is not uniquely determined to the cel current value Id, and two or more data values cannot be made equivalent to the cel current value Id.
[0024] Thus, in the flash EEPROM using the split-gate mold memory cell 101, only a field with much change of the cel current value Id can be used to change of the floating-gate potential Vfg on the occasion of multiple-value-izing.
(Stack TOGETO mold) The cross-section structure of the stack TOGETO mold memory cell 201 is shown in drawing 9 .
[0025] The N type source S and Drain D are formed on the P type single crystal silicon substrate. On the channel CH pinched by Source S and Drain D, the floating gate FG is formed through the 1st insulator layer 203. The control gate CG is formed through the 2nd insulator layer 204 on the floating gate FG. A floating gate FG and the control gate CG are accumulated without shifting mutually. Therefore, Source S and Drain D take symmetry structure to each gates FG and CG and Channel CH.
[0026] The whole flash EEPROM 221 configuration which used the stack TOGETO mold memory cell 201 for drawing 10 is shown. In a flash EEPROM 221, it is the following points to differ from the flash EEPROM 121 using the split-gate mold memory cell 101 shown in drawing 6 R> 6.
[0027] (1) As for the memory cell array 122, two or more memory cells 201 are arranged in the shape of a matrix.
(2) The source S of each memory cell 201 arranged in the direction of a train is connected to common bit line BLa-BLz.
(3) The drain D of all the memory cells 201 is connected to the common drain line DL. The common drain line DL is connected to the common drain line bias circuit 222. The common drain line bias circuit 222 controls the potential of the common drain line DL corresponding to each mode of operation to carry out a postscript. Actuation of the common drain line bias circuit 222 is controlled by the control core circuit 132.
[0028] By the way, in this specification, the name of the source S in the split-gate mold memory cell 101 and the stack TOGETO mold memory cell 201 and Drain D determines read-out actuation as a base, and the one where potential is higher is made to call the source the one where a drain and potential are lower in read-out actuation. And also in write-in actuation or elimination actuation, it is made the same as it in read-out actuation about the name of Source S and Drain D.
[0029] Next, each mode of operation (washout mode, a write mode, read-out mode) of a flash EEPROM 221 is explained with reference to drawing 11 .
(a) In washout mode washout mode, it changes all bit line BLa-BLz into an opening condition, and potential of all the word lines WLm is made into a grand level. The common drain line bias circuit 222 impresses 12V to the drain D of all the memory cells 201 through the common drain line DL.
[0030] Consequently, FN tunnel current flows, the electron in a floating gate FG is drawn out to Drain D side, and elimination of the data indicated by the memory cell 201 is performed. This elimination actuation is performed to all the memory cells 201 connected to the selected word line WLm. In addition, elimination actuation (block elimination) can also be performed so much to all the memory cells 201 connected to each of that word line by choosing two or more word line WLa-WLz as coincidence.
[0031] (b) In a write mode write mode, 12V are supplied to the word line WLm connected to the control gate CG of the selected memory cell 201, and potential of other word line (non-choosing word line) WLa-WLl and WLn-WLz is made into a grand level. 5V are supplied to the bit line BLm connected to the source S of the selected memory cell 201, and potential of other bit line (non-choosing bit line) BLa-BLl and BLn-BLz is made into a grand level. The common drain line bias circuit 222 holds the drain D of all the memory cells 201 to a grand level through the common drain line DL.
[0032] Then, the potential of a floating gate FG is raised by coupling from the control gate CG, and the hot electron generated near the source S is poured in to a floating gate FG. Consequently, a charge is accumulated in the floating gate FG of the selected memory cell 201, and 1-bit data are written in and memorized.
(c) In read-out mode read-out mode, 5V are supplied to the word line WLm connected to the control gate CG of the selected memory cell 201, and potential of other word line (non-choosing word line) WLa-WLl and WLn-WLz is made into a grand level. Potential of all bit line BLa-BLz is made into a grand level. The common drain line bias circuit 222 impresses 5V to the drain D of all the memory cells 201 through the common drain line DL.
[0033] Consequently, like the case of the split-gate mold memory cell 101, the direction of the memory cell 201 of an elimination condition writes in the current (cel current) which flows from Drain D to Source S, and it becomes larger than the memory cell 201 of a condition. Therefore, each memory cell 201 can be made to memorize binary [of the data value "1" of an elimination condition, and the data value "0" of a write-in condition].

[0034] By the way, multiple-value memory is proposed also by the flash EEPROM using the stack TOGETO mold memory cell 201. The potential Vfg of a floating gate FG and the property of the cel current value Id in the stack TOGETO mold memory cell 201 are shown in drawing 12 . In addition, the floating-gate potential Vfg is the potential of the floating gate FG to Source S.

[0035] In the SUTAKKUTOGE-TO mold memory cell 201, since it is put without a floating gate FG and the control gate CG shifting mutually, the channel [directly under] CH of the control gate CG does not function as constant resistance like the split-gate mold memory cell 101, but it has only the function of a transistor. Therefore, as for the cel current value Id, the floating-gate potential Vfg serves as zero in the field of under the threshold voltage Vth (=1V) of a memory cell 201. And if the floating-gate potential Vfg exceeds threshold voltage Vth, the cel current value Id will become large in proportion to the floating-gate potential Vfg.

[0036] Therefore, if potential Vfgw is controlled by adjusting the operating time and controlling the amount of charges of a floating gate FG also by the stack TOGETO mold memory cell 201 in write-in actuation, the floating-gate potential Vfg is controllable. Consequently, the cel current value Id in read-out actuation can be set as arbitration. Then, as shown in drawing 12 , the cel current value Id matches [the field of under 40microA / the field of under 80microA] the field of under 160microA with a data value "00" for the field of under 120microA a data value "01" and more than 120microA a data value "10" and more than 80microA a data value "11" and more than 40microA, respectively. And in write-in actuation, the operating time is adjusted so that the floating-gate potential Vfg (= Va, Vb, Vc, Vd) may become a value corresponding to said each cel current value Id (= 40 80,120,160microA). If it does in this way, one memory cell 201 can be made to memorize the data of four values (= 2 bits).

[0037] However, in the stack TOGETO mold memory cell 201, even when drawing out a charge from a floating gate FG in elimination actuation, and the charge was extracted too much superfluously and the predetermined electrical potential difference (=0V) for making memory **** 201 into an OFF state is impressed to the control gate CG, Channel CH will turn on. Consequently, a memory cell 201 is always turned on, a cel current flows also in the state of the standby which does not perform each mode of operation (washout mode, a write mode, read-out mode), and the so-called problem of superfluous elimination it becomes impossible to read all the right data values of the memory cell which makes a bit line common arises. Therefore, it is not desirable to use the field of superfluous elimination for a data storage.

[0038] Also in read-out actuation, the sum of the potential Vfgc produced by coupling with the control gate CG and the potential Vfgw produced with the charge accumulated in the floating gate FG determines the potential of a floating gate FG (Vfg=Vfgc+Vfgw). That is, in read-out actuation, the field (Vfg-Vfgc=Vfgw>Vth) where the value which deducted Vfgc from the floating-gate potential Vfg exceeds threshold voltage Vth serves as superfluous elimination in the condition (Vfgc=5V) that the potential of a floating gate FG is raised by 5V by coupling from the control gate CG. That is, when Vfgc is 5V, the field beyond 6V serves as [the floating-gate potential Vfg] superfluous elimination.

[0039] Moreover, if each value of data is made equivalent to the cel current value Id, to change of the floating-gate potential Vfg, about the field where change of the cel current value Id is small, the floating-gate potential Vfg will not be determined uniquely and multiple-value-ization cannot be performed with the cel current value Id. That is, since the cel current value Id does not so much change [the floating-gate potential Vfg] to change of the floating-gate potential Vfg about the field below 1V, the floating-gate potential Vfg is not uniquely determined to the cel current value Id, and two or more data values cannot be made equivalent to the cel current value Id.

[0040] Thus, in the flash EEPROM using the stack TOGETO mold memory cell 201, on the occasion of multiple-value-izing, it cannot push down on change of the floating-gate potential Vfg, and only the field which is a field where change of the cel current value Id is big, and is not superfluous elimination can be used.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] If it is in the non-volatile semiconductor memory of this invention, since it is possible to secure sufficient read-out margin in readout actuation of the data of the memory cell which made the multiple-value data of binary or three values or more memorize, data can be read correctly.
[0081] Moreover, since multiple-value data can be distinguished without hardly passing a cel current, it is possible to supply non-volatile semiconductor memory with little power consumption. And package read-out can do many cels according to there being little power consumption, and improvement in a data read-out rate is possible.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In order to raise the degree of integration of the memory device per unit area, multiple-value-ization is one of the leading means, and is attracting attention in recent years. In a flash EEPROM, in case a multiple-value cell data is read, the cel current of a read-out cel is compared with a reference current value, and the data values (0, 1, 2, 3 , etc.) recorded on the memory cell are distinguished.
[0042] However, while comparing this reference current with a cel current and having distinguished the record data value, it is required to continue passing the current before and behind 100microper one cel A, and the increment in power consumption is not escaped. Moreover, the more it multiple-value-izes a memory cell, the more, many reference current values for comparing with each value currently recorded must be prepared, the count of a comparison with a reference current value increases, the read-out time amount per cel becomes long, and there is a problem which cannot respond to improvement in the speed.
[0043] On the other hand, in order to carry out write-in read-out of data to stability correctly and to prevent incorrect writing and incorrect read-out, it is desirable to prepare sufficient margin (large tolerance) in the range of the floating-gate potential Vfg corresponding to each data value of a multiple value and the range of the cel current value Id. However, as described above, by the flash EEPROM of a type, change of the cel current value Id can use only a big field to change of the floating-gate potential Vfg on the occasion of multiple-value-izing conventionally. Therefore, it is difficult to take sufficient margin for the range of the floating-gate potential Vfg corresponding to each data value of a multiple value, and the cel current value Id.
[0044] For example, in the split-gate mold memory cell 101 shown in drawing 8 , the range of the cel current value Id corresponding to each data value is 40microA, and the range of the floating-gate potential Vfg corresponding to 0.5V and a data value "01" in the range of the floating-gate potential Vfg corresponding to a data value "10" is 1V. Moreover, in the stack TOGETO mold memory cell 201 shown in drawing 12 , the range of the cel current value Id corresponding to each data value is 40microA, and the range of the floating-gate potential Vfg is 1.25V.
[0045] Thus, if the range of the floating-gate potential Vfg corresponding to each data value is narrow, in write-in actuation, there are few margins, it becomes difficult to set up the floating-gate potential Vfg in tolerance correctly, and since there are few margins, incorrect read-out will tend to occur also in read-out actuation. This problem appears more notably as multiple-value-ization progresses, and in an octal or 16 values, margin reservation of write-in read-out actuation becomes still more difficult [the part to which the range of the floating-gate potential Vfg corresponding to each data value of a multiple value and the range of the cel current value Id become narrow] compared with the case of four values.
[0046] If supply voltage is raised only for the purpose of securing a margin on the other hand, the upper limit of Vfg is raised and the upper limit of a cel current value is raised, in the case of read-out, a sense amplifier will detect the data value of a cel for much more currents with a sink, and the problem of the above-mentioned increment in power consumption will be promoted further. It is made in order that this invention may solve the above-mentioned trouble, and the purpose is in offering the non-volatile semiconductor memory which can secure read-out margin with it in read-out actuation. [small and power consumption and] [sufficient]

[Translation done.]

MEANS

[Means for Solving the Problem] It has the memory cell which consists of Source S, and Drain D and Channel CH if it is in the non-volatile semiconductor memory of claim 1, and since it begins to impress an electrical potential difference to the control gate CG in case the data currently recorded on the floating gate FG are read, said memory cell carries out counting of the time amount taken to actually begin to pass a cel current, and distinguishes a record data value by the size of these enumerated data. [a floating gate FG, the control gate CG, and]
[0048] That is, counting of the time amount which takes read-out of data for the potential of the floating gate to rise and for a read-out memory cell to actually begin to pass a cel current since an electrical potential difference begins to be impressed to a floating gate FG is carried out. for example, this recorded time amount -- 50ns or more, "2" can be distinguished for "1" and less than 150ns 100ns or more, and record data can be distinguished [less than 50ns / "0" and less than 100ns] for less than 200ns 150ns or more by "3", then the size of time amount by which counting was carried out.
[0049] Moreover, if it is in the non-volatile semiconductor memory of claim 2 It is what has the memory cell which consists of Source S, and Drain D and Channel CH. [a floating gate FG, the control gate CG, and] In case the data currently recorded on the floating gate FG are read, an electrical potential difference is impressed to the control gate CG of a reference cel. Since this reference cel begins to pass a cel current, counting of the time amount until said memory cell begins to pass a cel current is carried out, and a record data value is distinguished by the size of these enumerated data.
[0050] That is, since an electrical potential difference begins to be impressed to a floating gate FG, the potential of the floating gate FG of a reference cel rises, and since a reference cel begins to pass a cel current, read-out of data carries out counting of the time amount until the memory cell which carries out the control gate CG to a reference cel in common begins to pass a cel current. By carrying out like this, the time variation which the channel generation resulting from process dispersion, such as gate processing, takes can be effectively removed from the error of data detection.
[0051] and these enumerated data -- for example, 0 or 50ns or more, less than 150ns can be distinguished 1,100ns or more, and a record data value can be distinguished [less than 50ns / less than 100ns] for less than 200ns 2,150ns or more by 3, then the size of time amount by which counting was carried out. Moreover, if it is in the non-volatile semiconductor memory of claim 3, it is controlling the amount of the charge accumulated in said floating gate FG, and multiple-value data are made to record on said memory cell, in the case of read-out of data, an electrical potential difference is impressed to the control gate CG by the constant current power supply, and the potential Vfg of a floating gate FG is controlled by coupling from the control gate CG.
[0052] That is, in read-out mode, the amount of the current which flows into the control gate CG from a constant current power supply is adjusted, and it controls so that the potential R/C per time amount of the control gate CG becomes small. Moreover, if it is in the non-volatile semiconductor memory of claim 4, it is controlling the amount of the charge accumulated in said floating gate FG, and multiple-value data are made to record on said memory cell, in the case of read-out of data, an electrical potential difference is impressed to the control gate CG through the circuit where a time constant is large, and the potential Vfg of a floating gate FG is controlled by coupling from the control gate CG.
[0053] That is, in read-out mode, when a time constant with strong resistance lets the circuit beyond about 1000ns and it pass and carries out electrical-potential-difference impression, it controls so that the potential R/C per time amount of the control gate CG becomes small. moreover -- a claim -- five -- a non-volatile -- semiconductor memory -- it is -- if -- being according to claim 3 or 4 -- a non-volatile -- semiconductor memory -- setting -- the time -- a constant current power supply -- control -- the gate -- CG -- an electrical potential difference -- impressing -- things -- replacing with -- a constant current source -- a drain -- D -- or -- the source -- S -- an electrical potential difference -- impressing -- a drain -- D -- or -- the source -- S -- from -- coupling -- a floating gate -- FG -- potential -- Vfg -- controlling -- a thing -- it is .
[0054] Moreover, if it is in the non-volatile semiconductor memory of claim 6, in non-volatile semiconductor memory according to claim 3 or 4, a time constant replaces with impressing an electrical potential difference to the control gate CG through a large circuit, impresses an electrical potential difference to Drain D or Source S through the circuit where a time constant is large, and controls the potential Vfg of a floating gate FG by Drain D or coupling from Source S.
[0055] Moreover, if it is in the non-volatile semiconductor memory of claim 7, the number machine of hour meters which carries out counting of the time amount with a clock is formed. Moreover, if it is in the non-volatile semiconductor memory of claim 8, the control circuit which distinguishes a record data value by the size of gate time is prepared.
[0056]

[Embodiment of the Invention] Below, the operation gestalt which materialized this invention is explained according to a drawing.
(The 1st operation gestalt) The 1st operation gestalt which materialized this invention is explained based on a drawing. The whole flash EEPROM configuration which used the split-gate mold memory cell 101 of this operation gestalt for drawing 1 is shown. One memory cell 101 can be made to memorize the data beyond 4 values (= 2 bits) in this operation gestalt.
[0057] In drawing 1 , it is the point of the following related with read-out that a flash EEPROM 1 differs from the conventional flash EEPROM 121 shown in drawing 6 . There are not the conventional example and a difference about the part about washout mode and a write mode.
(1) In read-out mode, in case an electrical potential difference is impressed to Drain D by the column decoder, carry out using a constant current power supply 2. In other modes, this constant current power supply 2 is bypassed, and electrical-potential-difference impression is performed.
[0058] (2) In read-out mode, the number machine 3 of hour meters is used as an output buffer. This forms the counter 2 bits or more for every bit line, and carries out counting of the time difference with the time of day when it reads at with the time of day which impressed the electrical potential difference with the common clock 4, and a memory cell begins to pass a current. The cross-section structure of the split-gate mold memory cell in this operation gestalt is the same as that of what was shown in drawing 5 . A constant current source 2 is connected to Drain D in the case of read-out, and it raises the potential of Drain D with time amount. At this time, the potential Vfg of a floating gate FG also rises with time amount by coupling from Drain D. If the potential Vfg of a floating gate exceeds the threshold voltage Vth of a memory cell, Channel CH will be generated under a floating gate and a cel current will begin to flow.
[0059] With this operation gestalt, since the capacity Ccf of the control gate CG and a floating gate FG is very small compared with the capacity of Drain D and a floating gate FG, and the capacity of a floating gate FG and a substrate, it disregards this and continues explanation below. It reads with Drain D and capacity between Cdf, a floating gate FG, and a substrate (just before channel generation) is set to Cfs for the capacity between the floating gates FG of a memory cell. By coupling with Drain D Set to QdfQfs positive charge accumulated in capacity Cdf and Cfs, respectively, and if the potential difference of Vfg, a floating gate, and a substrate is set to Vfs for the potential of Vd and a floating gate, the potential of Drain D A channel is generated when the potential Vfg of a floating gate FG becomes equal to Vth like following the (1) type.
[0060]
Vfg=Vth=Vfs=Vd-Vdf ---(1)
In this invention, the time amount t which this took is measured and the written-in data value is distinguished. That is, it is an electron (negative charge) to a floating gate FG by the writing of data. - When a channel is generated, it becomes Vdf=(Qw+Qdf)/CdfVfs=Vth=Vfg=Qfs/CfsQdf=Qfs, therefore Vd=Vdf+Vth=(Qw+Qdf)/Cdf+Qfs/Cfs, and compared with the case where there is no are recording of a charge in floating-gate CG, where Qw is accumulated, if only Qw/Cdf does not give big potential to the control gate CG, channel generation will not take place but channel generation will take time amount only at this rate. For this reason, if positive charge is given to Drain D in proportion to time amount and the potential of the control gate CG is raised using the constant current power supply 2, the amount of the electron accumulated by data writing will be uniquely detected by the time amount which channel generation takes.
[0061] for example, the case where the data of four values are distinguished -- time amount t<a a case -- "00" and a<t<b it is -- a case -- "01" and b<t<c it is -- a case -- "10" and t>b it is -- the case specifies beforehand that it calls it "11" (a<b<c<d), and carries out a comparison test in the control core circuit 132.
(The 2nd operation gestalt) The 2nd operation gestalt which materialized this invention is explained based on a drawing.
[0062] In this operation gestalt, differing from the 1st operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 1st operation gestalt.
(1) In read-out mode, in case an electrical potential difference is impressed to Drain D by the column decoder 124, as it replaces with a constant current power supply 2 and is shown in drawing 2 , it lets the circuit 5 where a time constant is big pass, and carry out using the usual constant voltage power supply 6. In other modes, the circuit 5 where this time constant is big is bypassed, and electrical-potential-difference impression is performed.
[0063] Namely, output voltage of a constant voltage power supply V0 and time constant of a circuit 5 tau Then, the drain electrical potential difference Vd in read-out mode becomes Vcg = V0[1-exp(- t/tau)] (for a time constant and t, time amount and V0 are [tau] supply voltage). Big Resistance R and capacity C are contained in the circuit 5 where a time constant is big, and the time constant has become more than 1000ns or it. Thus, if an electrical potential difference is impressed to Drain D through a circuit with a big time constant, the power surge per time amount can be made small, and a gradually big electrical potential difference will be impressed to Drain D with the passage of time. Thus, by using the circuit 5 where a time constant is big, the voltage buildup rate of the drain D per time amount can be made small, before a read-out memory cell reaches threshold voltage so that there are many electrons accumulated in the floating gate by data writing like the 1st operation gestalt in this case, time amount can be taken mostly, and the data value written in by carrying out counting of this time amount can be distinguished.
(The 3rd operation gestalt) The 3rd operation gestalt which materialized this invention is explained below.
[0064] In this operation gestalt, differing from the 1st operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 1st operation gestalt.
(1) In read-out mode, only the number of the cel read to coincidence forms the counter 2 bits or more in the number machine

3 of hour meters used as an output buffer, and carry out counting of the time difference of the time of day which impressed the electrical potential difference to the drain D of a read-out memory cell, and the time of day when a read-out memory cell begins to pass a current to it using the signal of the common clock 4.
[0065] Therefore, since it is sufficient for the number of a counter if only the number of the input output line of data is prepared, and it does not need to attach a counter to all bit lines, a circuit is made as for it to an abbreviation and a small scale.
(The 4th operation gestalt) The 4th operation gestalt which materialized this invention is explained based on a drawing. In this operation gestalt, differing from the 1st operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 1st operation gestalt.
[0066] (1) Prepare every one reference cel REFa-REFz for detecting a reference sign for every word line in drawing 1 . For example, a cel connected to the bit line BLz is made into reference cel REFa-REFz. From the time of day when this cel began to pass a cel current, a read-out memory cell carries out counting of the time difference by the time of day which begins to pass a cel current with the number vessel 5 of hour meters using the signal of a clock 4.
[0067] When it carries out like this, read-out of data by coupling from Drain D An electrical potential difference is impressed to a floating gate FG, and the potential of the floating gate FG of a reference cel rises. By the signal which began to pass a cel current, the read-out memory cell to which a reference cel starts counting with a clock by the signal which began to pass a cel current, and carries out the control gate CG to a reference cel in common measures a stop and two kinds of this time difference, and records counting with a clock. In this way, even if there is process dispersion, such as gate processing, the time variation which the channel generation resulting from this takes can be effectively removed from the error of data detection.
(The 5th operation gestalt) The 5th operation gestalt which materialized this invention is explained based on a drawing.
[0068] The whole flash EEPROM configuration which used the stack TOGETO mold memory cell 201 of this operation gestalt for drawing 3 is shown. One memory cell 201 can be made to memorize the data beyond 4 values (= 2 bits) in this operation gestalt. In drawing 3 , it is the point of the following related with read-out that a flash EEPROM 2 differs from the conventional flash EEPROM 221 shown in drawing 10 . About the part about washout mode and a write mode, it is the same as that of the conventional example.
[0069] (1) In read-out mode, in case an electrical potential difference is impressed to the control gate by the low decoder 123, carry out using a constant current power supply 2. In other modes, this constant current power supply 2 is bypassed, and electrical-potential-difference impression is performed.
(2) In read-out mode, the number machine 3 of hour meters is used as an output buffer. This forms the counter 2 bits or more for every bit line, and carries out counting of the time difference with the time of day when it reads at with the time of day which impressed the electrical potential difference with the common clock 4, and a memory cell begins to pass a current.
[0070] The cross-section structure of the stack TOGETO mold memory cell in this operation gestalt is the same as that of what was shown in drawing 9 . A constant current power supply 151 is connected with the control gate CG in the case of read-out, and it raises the potential of the control gate CG with time amount. At this time, the potential Vfg of a floating gate FG also rises with time amount by coupling from the control gate CG. If the potential Vfg of a floating gate exceeds the threshold voltage Vth of a memory cell 201, Channel CH will be generated and a cel current will begin to flow.
[0071] It reads with the control gate CG and capacity between Ccf, a floating gate FG, and a substrate (just before channel generation) is set to Cfs for the capacity between the floating gates FG of a memory cell. By coupling with the control gate CG Positive charge accumulated in capacity Ccf and Cfs is set to QcfQfs, respectively. A channel is generated, when it becomes about the potential of Vcg and a floating gate in the potential of the control gate and Vfs, then the potential Vfg of a floating gate FG become equal to Vth like following the (2) type about the potential difference of Vcf, a floating gate, and a substrate in the potential difference of Vfg, the control gate, and a floating gate.
[0072]
Vfg=Vth=Vfs=Vcg-Vcf ---(2)
In this invention, the time amount t which this took is measured and the written-in data value is distinguished. That is, it is an electron (negative charge) to floating-gate CG by the writing of data. - When a channel is generated, it becomes Vcf=(Qw+Qcf)/CcfVfs=Vth=Vfg=Qfs/CfsQcf=Qfs, therefore Vcg=Vcf+Vth=(Qw+Qcf)/Ccf+Qfs/Cfs, and compared with the case where there is no are recording of a charge in floating-gate CG, where Qw is accumulated, if only Qw/Ccf does not give big potential to the control gate CG, channel generation will not take place but channel generation will take time amount only at this rate. For this reason, if positive charge is given to the control gate CG in proportion to time amount and the potential of the control gate CG is raised using the constant current power supply 2, the amount of the electron accumulated by data writing will be uniquely detected by the time amount which channel generation takes.
[0073] for example, the case where the data of four values are distinguished -- time amount t<a a case -- "00" and a<t<b it is -- a case -- "01" and b<t<c it is -- a case -- "10" and t>b it is -- the case specifies beforehand that it calls it "11" (a<b<c<d), and carries out a comparison test in the control core circuit 132.
(The 6th operation gestalt) The 6th operation gestalt which materialized this invention is explained based on a drawing.
[0074] In this operation gestalt, differing from the 5th operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 5th operation gestalt.
(1) In read-out mode, in case an electrical potential difference is impressed to the control gate FG by the low decoder 123, it lets the circuit 5 where the time constant shown in drawing 4 is big pass, and carry out using the usual constant voltage power

supply 6. In other modes, the circuit 5 where this time constant is big is bypassed, and electrical-potential-difference impression is performed.

[0075] That is, the control gate voltage [in / for the time constant of V0 and a circuit 5 / in the output voltage of a constant voltage power supply / tau, then read-out mode] Vcg becomes Vcg = V0[1-exp(- t/tau)] (for a time constant and t, time amount and V0 are [tau] supply voltage). Big Resistance R and capacity C are contained in the circuit 5 where a time constant is big, and the time constant has become more than 1000ns or it. Thus, if an electrical potential difference is impressed to Drain D through a circuit with a big time constant, the power surge per time amount can be made small, and a gradually big electrical potential difference will be impressed to Drain D with the passage of time. Thus, by using the circuit 5 where a time constant is big, the voltage buildup rate of the drain D per time amount can be made small, before a read-out memory cell reaches threshold voltage so that there are many electrons accumulated in the floating gate by data writing like the 5th operation gestalt in this case, time amount can be taken mostly, and the data value written in by carrying out counting of this time amount can be distinguished.

(The 7th operation gestalt) The 7th operation gestalt which materialized this invention is explained below.

[0076] In this operation gestalt, differing from the 5th operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 5th operation gestalt.

(1) In read-out mode, only the number of the cel read to coincidence forms the counter 2 bits or more in the number machine 3 of hour meters used as an output buffer, and carry out counting of the time difference of the time of day which impressed the electrical potential difference to the control gate CG of a read-out memory cell, and the time of day when a read-out memory cell begins to pass a current to it using the signal of the common clock 4.

[0077] Therefore, since it is sufficient for the number of a counter if only the number of the input output line of data is prepared, and it does not need to attach a counter to all bit lines, it omits a circuit and is made on a small scale.

(The 8th operation gestalt) The 8th operation gestalt which materialized this invention is explained based on a drawing. In this operation gestalt, differing from the 5th operation gestalt is the point of the following related with read-out. About other parts, it is the same as that of the 5th operation gestalt.

[0078] (1) Prepare every one reference cel REFa-REFz for detecting a reference sign for every word line in drawing 3 . For example, a cel connected to the bit line BLz is made into reference cel REFa-REFz. From the time of day when this cel began to pass a cel current, a read-out memory cell carries out counting of the time difference by the time of day which begins to pass a cel current with the number vessel 5 of hour meters using the signal of a clock 4.

[0079] When it carries out like this, read-out of data by coupling from the control gate CG An electrical potential difference is impressed to a floating gate FG, and the potential of the floating gate FG of a reference cel rises. By the signal which began to pass a cel current, the read-out memory cell to which a reference cel starts counting with a clock by the signal which began to pass a cel current, and carries out the control gate CG to a reference cel in common measures a stop and two kinds of this time difference, and records counting with a clock. In this way, even if there is process dispersion, such as gate processing, the time variation which the channel generation resulting from this takes can be effectively removed from the error of data detection.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the whole flash EEPROM block diagram using the split-gate mold memory cell in the operation gestalt of this invention.
[Drawing 2] It is drawing showing the big circuit and big constant voltage power supply of a time constant.
[Drawing 3] It is the whole flash EEPROM block diagram using the SUTAKKUTOGE-TO mold memory cell in the operation gestalt of this invention.
[Drawing 4] It is drawing showing the big circuit and big constant voltage power supply of a time constant.
[Drawing 5] It is the cross-section structure of a split-gate mold memory cell.
[Drawing 6] It is the whole flash EEPROM block diagram using the conventional split-gate mold memory cell.
[Drawing 7] It is the explanatory view of each mode of operation in the conventional flash EEPROM.
[Drawing 8] It is drawing showing the potential Vfg of a floating gate FG and the property of the cel current value Id in a split-gate mold memory cell.
[Drawing 9] It is drawing showing the cross-section structure of a stack TOGETO mold memory cell.
[Drawing 10] It is the whole flash EEPROM block diagram using the conventional stack TOGETO mold memory cell.
[Drawing 11] It is the explanatory view of each mode of operation in the conventional flash EEPROM.
[Drawing 12] It is drawing showing the potential Vfg of a floating gate FG and the property of the cel current value Id in a stack TOGETO mold memory cell.
[Description of Notations]
2 Constant Current Power Supply
3 The Number Machine of Hour Meters
4 Clock
5 Circuit Where Time Constant is Big
6 Constant Voltage Power Supply
101 201 Memory cell
132 Control Core Circuit

[Translation done.]

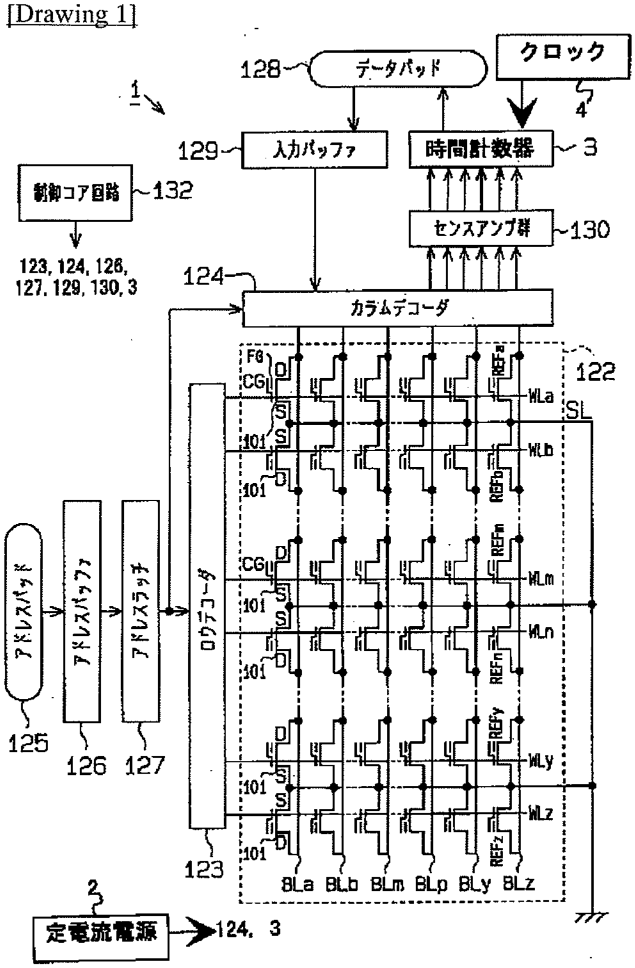
* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

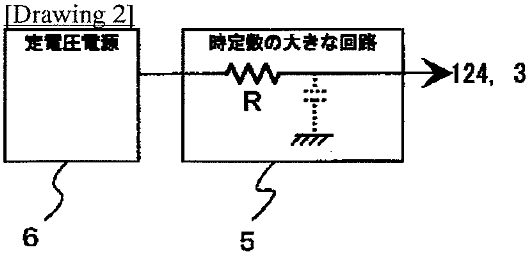
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

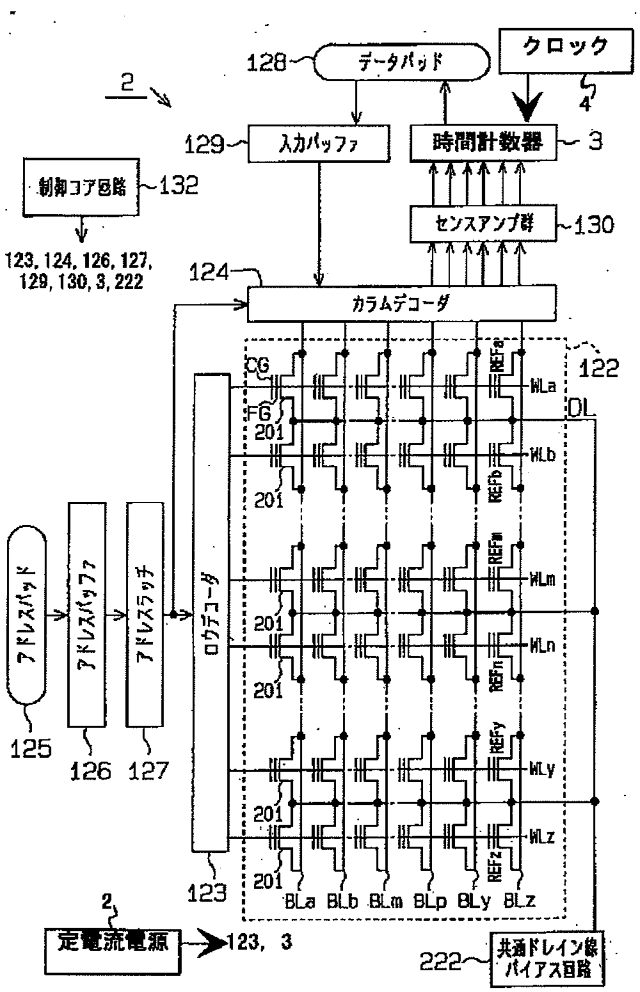
[Drawing 1]



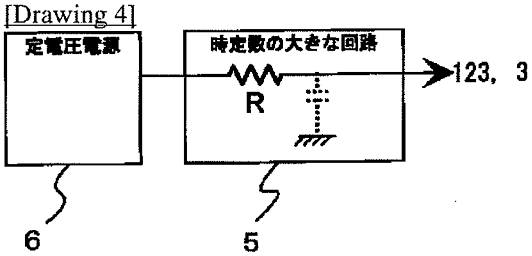
[Drawing 2]



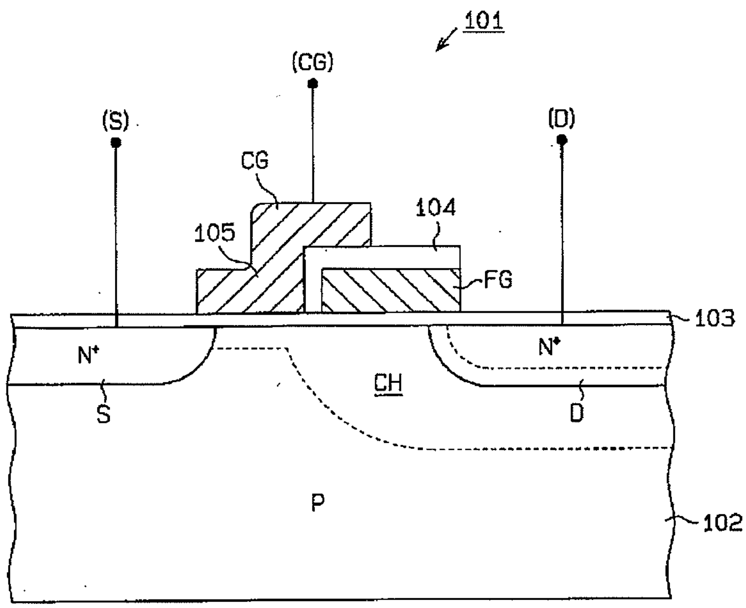
[Drawing 3]



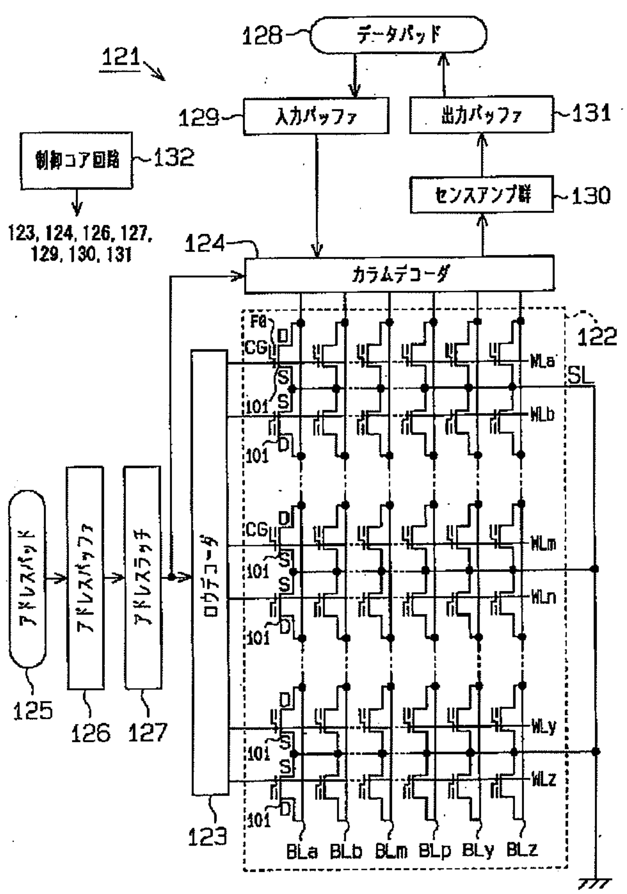
[Drawing 4]



[Drawing 5]



[Drawing 6]



[Drawing 7]

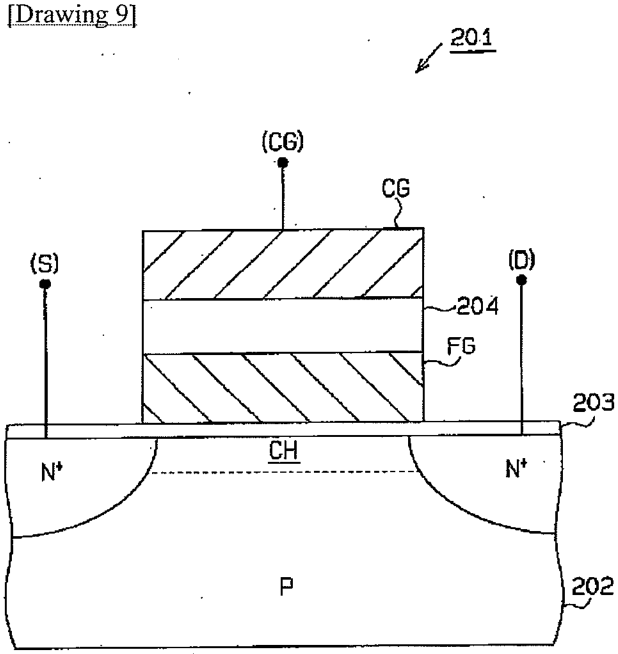
(a)

動作モード	書き込み	消去	読み出し	スタンバイ
ワード線WLm (制御ゲートCG)	1V	15V	5V	0V
ビット線BLm (ドレインD)	12V	0V	2.5V	0V
共通ソース線SL (ソースS)	0V	0V	0V	0V
基板102	0V	0V	0V	0V

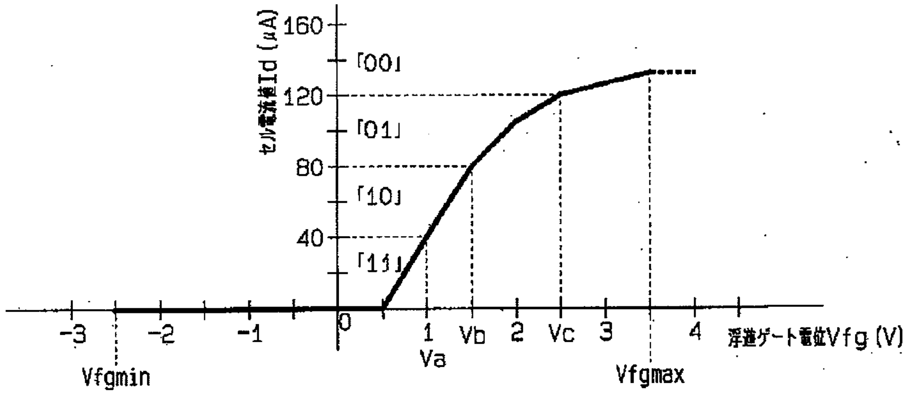
(b)

動作モード	書き込み	消去	読み出し	スタンバイ
ワード線WLm (制御ゲートCG)	1V	15V	5V	0V
ビット線BLm (ドレインD)	0V	0V	2.5V	0V
共通ソース線SL (ソースS)	12V	0V	0V	0V
基板102	0V	0V	0V	0V

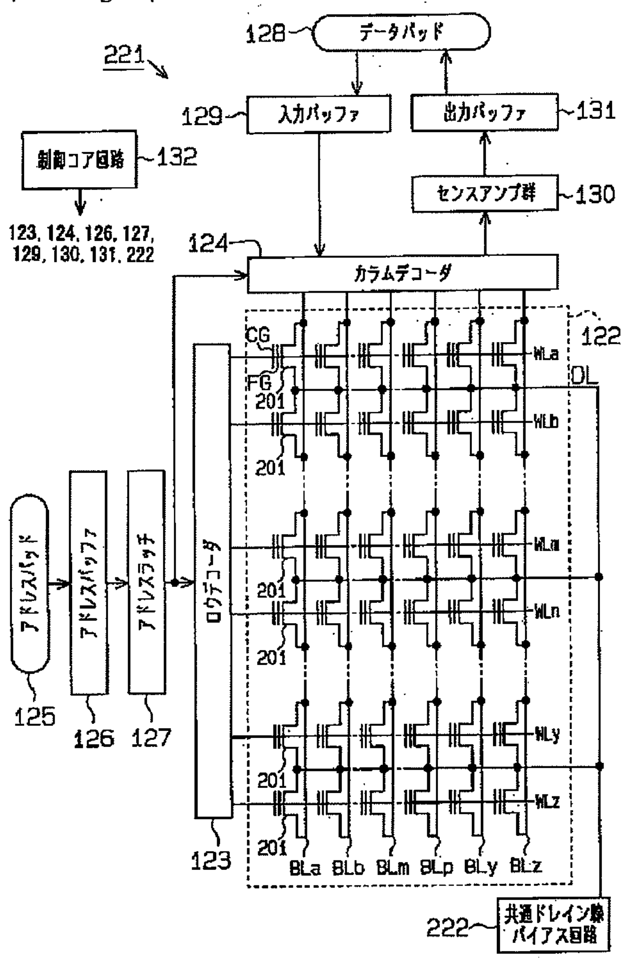
[Drawing 9]



[Drawing 8]



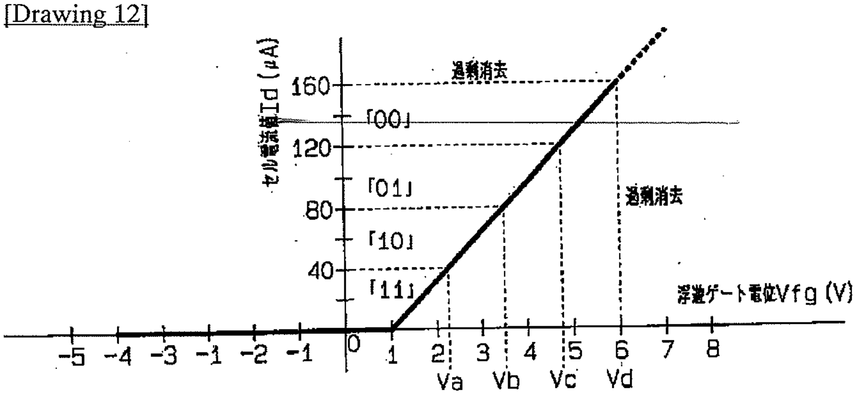
[Drawing 10]



[Drawing 11]

動作モード	書き込み	消去	読み出し	スタンバイ
ワード線WLm (制御ゲートCG)	12V	0V	5V	0V
共通ドレイン線DL (ドレインD)	0V	12V	5V	0V
ビット線BLm (ソースS)	5V	OPEN	0V	0V
基板202	0V	0V	0V	0V

[Drawing 12]



[Translation done.]